17CS34 COMPUTER ORGANIZATION

Question Bank:

# BASICSTRUCTURE OFCOMPUTERS

1. **List the steps needed to execute the machine instruction Add LOCA, R0 in terms of transfer between processor and the memory along with some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address initially in register PC. The first two steps might be expressed as:**
   * **Transfer the content of register PC to register MAR**
   * **Issue read command to the memory and then wait until it has transferred the requested word int register MDR.** [l1] [l3][l3][co1]
2. Explain performance measurement and the overall SPEC rating for the computer in a program suite [l2][co1]
3. **Describe the operational concepts between the processor and memory** [l1][co1]
4. **Explain the different functional units of a computer**. [l2][co1]
5. **Draw and explain the connection between memory and processor with the respective registers.** [l1] [l2] [co1]
6. With a neat diagram, discuss the operational concepts of a computer. [l2][co1]
7. Draw the connection between processor and memory and mention the functions of each component in the connection. [l1] [co1]
8. Write the difference between RISC and CISC processors. [l1] [l2] [co1]

# MACHINE INSTRUCTIONS AND PROGRAMS

1. **Define addressing modes. Give the details of different addressing modes.** [l1] [l2] [co2]
2. **Explain the role of stack and queues in computer programming equations** [l2] [co2]
3. Explain the shift and rotate operation with examples [l2] [co2]
4. **Explain logical shift and rotate instructions with examples**[l2] [co2]
5. **Define an addressing mode .Explain the following addressing modes, with example for each**
   1. **Index addressing mode**
   2. **Indirect addressing mode**
   3. **Relative addressing mode**
   4. **Auto decrement addressing mode** [l1] [l2] [co2]

1. With a neat diagram, describe the input and output operations [l1] [co2]
2. List the name, assembler syntax and addressing functions for the different addressing modes.

[l1] [co2]

1. Explain logical and arithmetic shift instructions with an example. [l2] [co2]
2. **Explain different rotate instructions.** [l2] [co2]
3. **List four types of operations to be performed by instructions in a computer. Explain with basic types of instruction formats to carry out C 🡨[A] + [B]** [l1] [l2] [co2]

# INPUT/OUTPUTORGANIZATION

1. **In a situation where multiple devices capable of initiating interrupts are connected to the processor, explain the implementation of interrupt priority, using individual INTER and INTA and a common INTR line to all devices**. (10 M) June 2012
2. Define the terms ‘cycle stealing and ‘block mode’. (2M) June 2012
3. What is bus arbitration? Explain different approaches to bus arbitration. (8M) June 2012
4. Define memory mapped I/O and I/O mapped I/O with examples (5M) Dec 2012
5. What are the different methods of DMA? Explain them in brief. (5M) Dec 2012
6. Explain how interrupt requests from several IO devices can be communicated to a processor through a single INTR line (10M) Dec 2012
7. With neat sketches, explain the various methods for handling multiple interrupt requests.

(12 M)June 2013

1. **Draw the arrangement of a single bus structure and brief about memory mapped I/O.**

(5M) Dec 2013

1. **Explain: i) Interrupt enabling; ii) Interrupt disabling; iii) Edge triggering, with respect to Interrupts.** (10M) Dec 2013
2. Draw the arrangement for bus arbitration using a daisy chain and explain. (5 M) Dec 2013
3. Explain the following wrt interrupts with diagrams. i. Vectored interrupt ii. Interrupt Nesting. iii. Simultaneous request
4. Explain the following terms:

i) Interrupt service routine ii) Interrupt latency iii) interrupt disabling. (6 M) June 2014

1. **Explain following methods of handling interrupts from multiple devices.**

**a. daisy chaining technique. b. Interrupt nesting/priority structure** (6 M) June 2018

1. What is an interrupt? With example illustrate the concept of interrupts. (6 M) Dec 2014
2. Explain in detail, the situations where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems? (8 M)Dec 2014
3. Briefly discuss the main phases involved in the operation of SCSI bus. (6M) June 2012
4. Explain tree structure of USB with split bus operation. (6M) June 2012
5. Explain with a neat block diagram, the hardware components needed for connecting a keyboard to a processor. (8M) June 2012
6. Explain the serial port and serial interface (6M)Dec 2012
7. Explain the architecture and protocols w.r.t. to USB (8M)Dec 2012
8. With a neat diagram,explain in detail the input interface circuit (10M) June 2013
9. List the functions of an I/O interface (3 M) June 2013
10. Discuss briefly the protocols of universal serial bus (7 M) June 2013
11. Explain the use of PCI bus in a computer system with necessary figure. (5 M) Dec2013
12. List the SCSI bus signals with their functionalities. (5 M) Dec2013
13. With a block diagram, explain how the printer is interfaced to the processor

(8 M) June 2014

1. Explain the architecture and addressing scheme of USB (8 M) June2014
2. Define two types of SCSI controller. (4M) June2014
3. Describe how a read operation is performed on a PCI bus. (10M) Dec2014
4. List the sequence of events that takes place when a processor sends a command to SCSI controller. (10M) Dec2014
5. With neat diagram explain how to interface printer to the processor. (8M June2018) 34.

# MEMORYSYSTEM

1. Explain the internal organisation of a 16 Megabits DRAM chip configured as 2MX8 cells. (8M)June 2012
2. Describe the principles of magnetic disk (6M)June 2012
3. With a block diagram, explain the direct and set associative mapping between cache and main memory (6M)June 2012
4. Draw a diagram and explain the working of 16 Megabits DRAM chip configured as 2MX8.Also explain as at how it can be made to work in fast page mode. (10M)Dec 2012
5. Briefly explain any four non-volatile memory concepts. (5M) Dec 2012
6. With figure analyse the memory hierarchy in terms of speed cost and size.(5M) Dec 2012
7. Briefly explain any two cache mapping functions. (6M)June 2013
8. With a neat diagram, explain the translation of a virtual address to a physical address.

(8M) June 2013

1. Discuss in detail any one feature of memory design that leads to improved performance of computer. (6M) June 2013
2. Draw for lK x 1memory chip with neat figure. (10M) Dec 2013
3. Show with diagram the memory hierarchy with respect to speed, size and cost.

(5M) Dec 2013

1. With a figure explain about direct mapping cache memory. (5M) Dec 2013
2. Explain direct memory mapping technique. (6 M)June 2014
3. What is virtual memory? With a diagram, explain how virtual memory address is translated. (8M)June 2014
4. Explain the working of 16-megabyte DRAM chip configured as 1M x 6 memory chip. (6 M) June 2014
5. Discuss the internal organization of a 2M x 8 asynchronous DRAM chip. (10M) Dec 2014
6. Describe the different mapping functions in cache. (10M) Dec 2014

# BASICPROCESSINGUNIT

* 1. List out the actions needed to execute the instruction ADD (R3), R1. Write and explain the sequence of control steps for the execution of the same. (10M)June 2012
  2. With a neat block diagram, explain hardwired control unit. Show the generation Zin and end control signals. (10M) June 2012
  3. Write and explain the control sequence for execution of an unconditional branch instruction. (10 M)Dec 2012
  4. Draw and explain multiple bus organization. Explain its advantages. (10M)Dec2012
  5. Write down the control sequence for the instruction ADD R4, R5, R6 for three bus organisation. (4 M)June 2013
  6. With a neat sketch, explain the organisation of a micro programmed control unit. (8M) June 2013
  7. With an example, explain the field coded micro instructions. (8M) June 2013
  8. Draw and explain the single-bus organization of the data path inside a processor. (10 M)Dec 2013
  9. Write the control sequence for an un-conditional branch instruction. (5 M)Dec 2013
  10. Draw the block diagram of the control unit organization and describe in brief. (5M)Dec 2013
  11. With a diagram, explain typical single bus processor data path. (8 M)June 2014
  12. Explain with neat diagram, the basic organization of a microprogrammed control unit. (8 M) June 2014
  13. Differentiate hardwired and micro programmed control unit. (4 M) June 2014
  14. Explain the three - bus organization of the processor. (8 M)Dec 2014
  15. Discuss the organization of hardwired control unit. (8 M)Dec 2014
  16. Write the micro-routine for the instruction Add - (Rsrc), Rdst. (4 M)Dec 2014
  17. What is embedded systems? Explain with examples. (10 M)
  18. Explain the organization of a simple microcontroller and discuss some features that may be used in practice. (10 M)
  19. Explain the structure of general purpose multiprocessor in detail. (10 M)